Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 to 8 (canceled).

Claim 9 (previously presented): The node controller of claim 18, further comprising:

command queues coupled to the logic engine, the command queues operable to store logic control blocks which can be processed by the logic engine.

Claims 10 to 12 (canceled).

Claim 13 (previously presented): The node controller of Claim 18, wherein the node controller is implemented as an integrated circuit device.

Claims 14 and 15 (canceled).

Claim 16 (currently amended): The node controller of Claim 9, further comprising:

a producer register operable to specify a first address of a command queue; and

a consumer register operable to specify a second address of [[a]] the command queue.

Claim 17 (canceled).

Claim 18 (currently amended) A node controller for a node in a data storage system having at least two nodes, the node comprising a computer-memory complex, the node controller distinct and separate from the computer-memory complex, and an input/output bus, the computer-memory complex comprising a central processing unit (CPU), a system memory, and a controller coupling the CPU and the system memory to the input/output bus, the node controller providing control for data transfer through the node, the node controller being operable to be programmed by the computer-memory complex, the node controller comprising:

a memory controller operable to interface the node controller with (1) a cluster memory that stores data being transferred through the node, and (2) a link coupled to another node controller in another node of the data storage system;

an input/output bus interface operable to interface the node controller with the input/output bus, at least one host device, and at least one storage device;

a logic engine coupled to (1) the memory controller, (2) the link, and (3) the input/output bus interface;

wherein in a first type of data transfer, the logic engine performs a logic operation to a plurality of data from one of a plurality of data sources in the data storage system and writes the result of the logic operation to one of a plurality of data destinations in the data storage system, the data sources comprising the cluster memory and the input/output bus interface, the data destinations comprising the cluster memory, the link, and the input/output bus interface, the logic operation being used to calculate a parity data for writing a full or a partial RAID stripe or to reconstruct a lost data using the parity data.

Claim 19 (previously presented): The node controller of claim 18, wherein in a second type of data transfer, the input/output bus interface writes a data into the cluster memory and in response the logic engine copies the data to the another node via the link.

Claim 20 (canceled).

Claim 21 (previously presented): The node controller of claim 18, wherein the input/output bus interface comprises a peripheral component interconnect (PCI) control interface and the input/output bus comprises a PCI bus.

Claim 22 (previously presented): The node controller of claim 21, wherein the computer-memory complex manages the PCI bus.

Claim 23 (previously presented): The node controller of claim 22, wherein the computer-memory complex supports a service selected from the group consisting of a HTTP service, a NFS service, and a CIFS service.

Claim 24 (currently amended): The node controller of claim 18, wherein the computer-memory complex is not burdened with temporarily storing data being transferred through the node in ~~the computer-memory complex~~ the system memory.

Claim 25 (previously presented): The node controller of claim 18, wherein the logic operation comprises an XOR operation.

Claims 26 to 28 (canceled).

Claim 29 (currently amended): A node in a data storage system comprising at least two nodes, the node comprising:

an input/output bus coupled to at least one host and at least one storage device;

a computer-memory complex, comprising:

a central processing unit (CPU);

a system memory storing information for controlling data transfer through the node; and

a controller coupling the CPU and the system memory to the input/output bus; and

a node controller distinct and separate from the computer-memory complex, the node controller providing ~~controller providing~~ control for data transfer through the node, the node controller being operable to be programmed by the computer-memory complex, the node controller comprising:

a memory controller operable to interface the node controller with a cluster memory of the node, the cluster memory storing data being transferred through the node;

an input/output bus interface operable to interface the node controller with the input/output bus;

a logic engine coupled to the memory controller, the input/output bus interface, and a link to another node of the data storage system;

wherein at least one of the host device and the storage device coupled to the input/output bus is able to read and write the cluster memory via the input/output bus,

the logic engine is able to transfer data from the cluster memory to the another node via the link, and the memory controller is able to receive data from the another node via the link.

Claims 30 to 34 (canceled).

Claim 35 (currently amended): The node of claim 29, wherein in a data transfer, the logic engine performs a logic operation on a plurality of data from at least one of the input/output bus and the cluster memory, and writes a result of the logic operation to at least one of the input/output bus, the cluster memory, and the link.

Claim 36 (previously presented): The node of claim 35, further comprising a command queue operable to store a logic control block to be processed by the logic engine, the logic control block specifying at least one data source and at least one data destination for the logic operation.

Claim 37 (previously presented): The node of claim 36, further comprising:

a producer register operable to specify a first address of the command queue; and

a consumer register operable to specify a second address of the command queue.

Claim 38 (previously presented): The node of claim 35, wherein the logic engine comprises an exclusive OR (XOR) engine.

Claim 39 (previously presented): The node of claim 38, wherein the XOR engine is used to calculate a parity data for writing a full or a partial RAID stripe.

Claim 40 (previously presented): The node of claim 38, wherein the XOR engine is used to reconstruct a lost data using a parity data.

Claim 41 (previously presented): The node of claim 29, wherein the node controller is implemented as an integrated circuit device.

Claim 42 (previously presented): The node of claim 29, wherein the input/output bus interface comprises a peripheral component interconnect (PCI) control interface and the input/output bus comprises a PCI bus.

Claim 43 (canceled).

Claim 44 (previously presented): The node of claim 29, wherein in a data transfer, the input/output bus interface writes a data into the cluster memory and in response the logic engine copies the data to the another node via the link.

Claim 45 (previously presented): The node of claim 29, wherein the computer-memory complex supports a service selected from the group consisting of a HTTP service, a NFS service, and a CIFS service.

Claim 46 (previously presented): The node of claim 29, wherein the computer-memory complex is not burdened with temporarily storing data being transferred through the node in the system memory.

Claim 47 (previously presented): The node of claim 29, further comprising:

another input/output bus interface operable to interface the node controller with another input/output bus coupled to the computer-memory complex and at least one of another host device and another storage device, wherein the computer-memory complex, the another host device, and the another storage device are able to read and write the cluster memory via the another input/output bus.

Claim 48 (currently amended): A node in a data storage system having at least two nodes for providing access to a data storage facility, the node comprising a computer memory complex, ~~and~~ a node controller distinct and separate from the computer-memory complex, and an input/output bus, the computer-memory complex comprising a central processing unit (CPU), a system memory, and a controller coupling the CPU and the system memory to [[an]] the input/output bus, the node controller providing control for data transfer through the node, the node controller being operable to be programmed by the computer-memory complex, the node controller comprising:

an input/output bus interface operable to interface the node controller with the input/output bus, at least one host device, and at least one storage device;

a memory controller operable to interface the node controller with a cache memory in the node;

one or more logic engines coupled to the input/output bus interface, to the memory controller, and to a link that can be coupled to another node in the data storage system;

wherein the node controller is arranged so that the computer-memory complex, the host device, and the storage device are able to access the node controller via the input/output bus so that the host device and the storage device are able to read and write the cache memory via the input/output bus; and

wherein the logic engine is able to transfer data from the cache memory to the another node in the data storage system via the link, and the memory controller is able to receive data from the another node in the data storage system via the link.

Claim 49 (currently amended): The node of claim 48, wherein the logic engine is operable to perform a logic operation in a data transfer on a plurality of data from at least one of the input/output bus and the cluster memory, and to write a result of the logic operation to at least one of the input/output bus, the cluster memory, and the link.

Claim 50 (currently amended): The node of claim 49, wherein the logic engine comprises an exclusive OR (XOR) engine.

Claim 51 (currently amended): The node of claim 49, the node controller further comprising a command queue operable to store a logic control block to be processed by the logic engine, the logic control block specifying [[a]] at least one data source and at least one data destination for the logic operation.

Claim 52 (previously presented): The node of claim 48, wherein the node controller is implemented as an integrated circuit device.

Claim 53 (previously presented): The node of claim 48, wherein the input/output bus interface comprises a peripheral component interconnect control interface and the input/output bus comprises a peripheral component interconnect bus.

Claim 54 (canceled).

Claim 55 (previously presented): The node of claim 51, the node controller further comprising:

a producer register operable to specify a first address of the command queue; and

a consumer register operable to specify a second address of the command queue.

Claim 56 (previously presented): The node of claim 48, wherein the node controller is arranged to send data written into the cache memory to the another node via the link.

Claim 57 (previously presented): The node of claim 48, wherein the computer-memory complex is arranged to support a service selected from the group consisting of a HTTP service, a NFS service, and a CIFS service.

Claim 58 (currently amended): The node of claim 48, wherein the computer-memory complex is not burdened with temporarily storing data being transferred through the node in ~~the computer-memory complex~~ the system memory.

Claim 59 (currently amended): The node of claim 50, wherein the ~~exclusive OR~~ XOR engine is arranged to calculate a parity data for writing a full or a partial RAID stripe.

Claim 60 (currently amended): The node of claim 50, wherein the ~~exclusive OR~~ XOR engine is arranged to reconstruct lost data using a parity data.

Claim 61 (previously presented): The node of claim 48, wherein the node controller is configured to act as a slave device.